

Seeds of SEED: **R-SAW**: New Side Channels Exploiting Read Asymmetry in MLC Phase Change Memories

Md Hafizul Islam Chowdhury¹, Ricard Ewetz¹, Amro Awad², and Fan Yao¹

¹Department of ECE
University of Central Florida
Florida

²Department of ECE
North Carolina State University
North Carolina

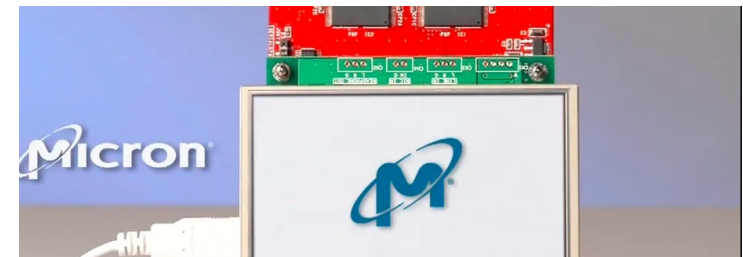
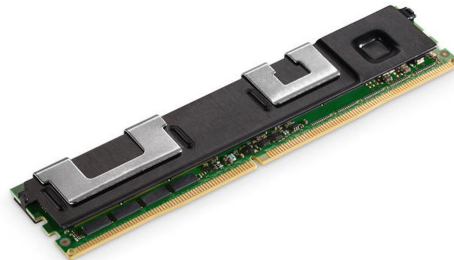
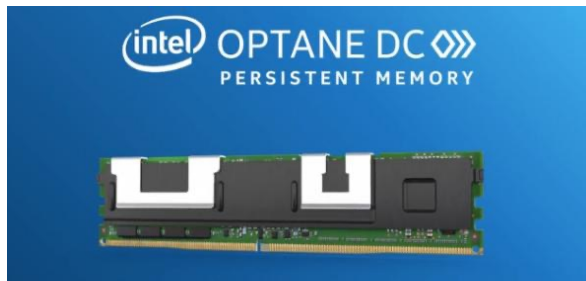
International Symposium on Secure and Private Execution Environment Design (SEED)
September 20 - 21, 2021

Microarchitecture Security

- ❖ Information security in hardware is a major concern.
 - Many microarchitectural components can be sources of leakage

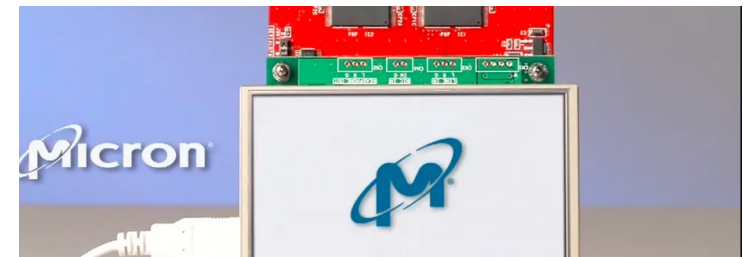
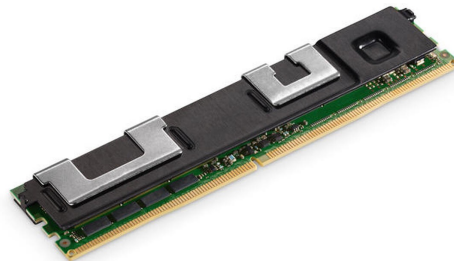
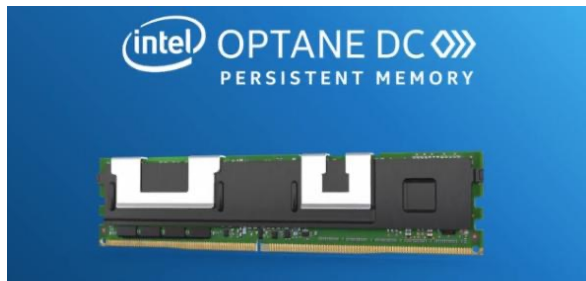
Microarchitecture Security

- ❖ Information security in hardware is a major concern.
 - Many microarchitectural components can be sources of leakage
- ❖ **Emerging technologies in memory subsystems (Non-volatile memory).**
 - PCM is the major contender for future main memory
 - Prior works focus on data integrity and remanence issues
 - **No prior studies of μ arch timing channels in PCM**



Microarchitecture Security

- ❖ Information security in hardware is a major concern.
 - Many microarchitectural components can be sources of leakage
- ❖ **Emerging technologies in memory subsystems (Non-volatile memory).**
 - PCM is the major contender for future main memory
 - Prior works focus on data integrity and remanence issues
 - **No prior studies of μ arch timing channels in PCM**



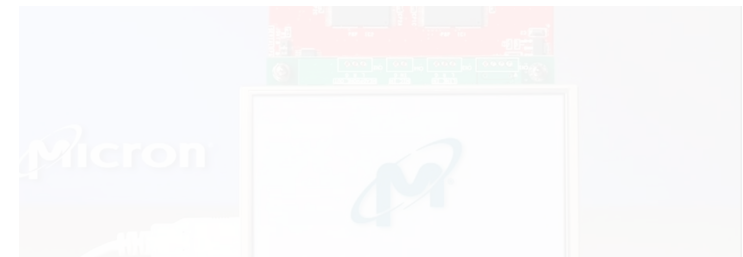
Lessons from past: Security needs to be understood by design, instead of an afterthought.

Microarchitecture Security

- ❖ Information security in hardware is a major concern.
 - Many microarchitectural components can be sources of leakage
- ❖ Emerging technologies in memory subsystems (Non-volatile memory).

This work

First investigation of information leakage vulnerabilities in Multi-level Cell PCM



Lessons from past:

Security needs to be understood by design, instead of an afterthought.

Background: MLC PCM

- ❖ PCM cells have wide range of resistance.



Figure: PCM cell resistance range

Background: MLC PCM

- ❖ PCM cells have wide range of resistance.
- ❖ **Single-level cell mode (SLC):** Each cell stores one bit.

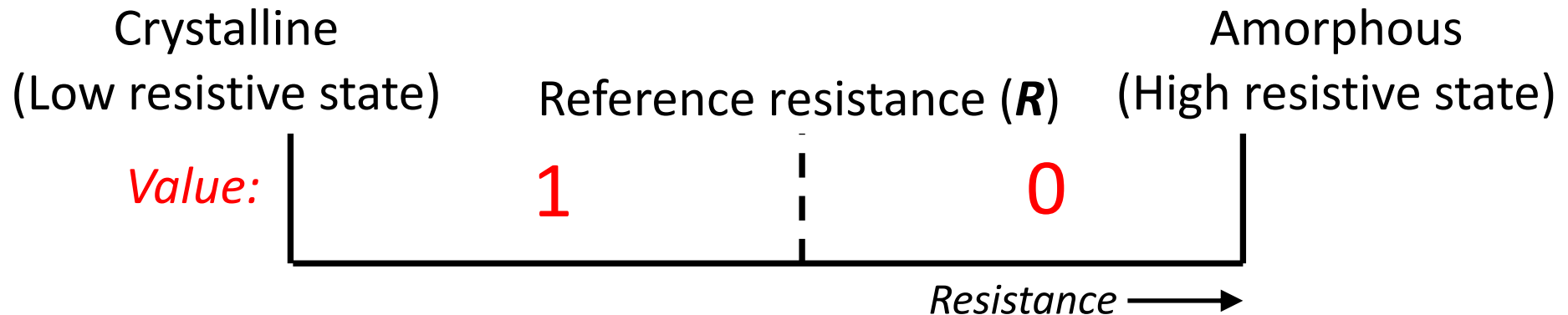


Figure: SLC PCM

Background: MLC PCM

- ❖ PCM cells have wide range of resistance.
- ❖ **Single-level cell mode (SLC):** Each cell stores one bit.
- ❖ **Multi-level cell mode (MLC):** Each cell stores two (or more) bits.

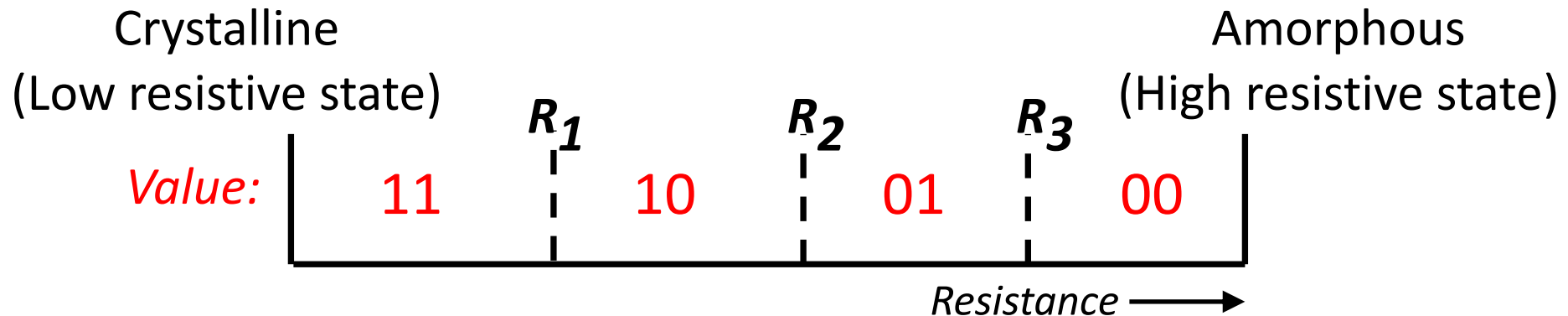
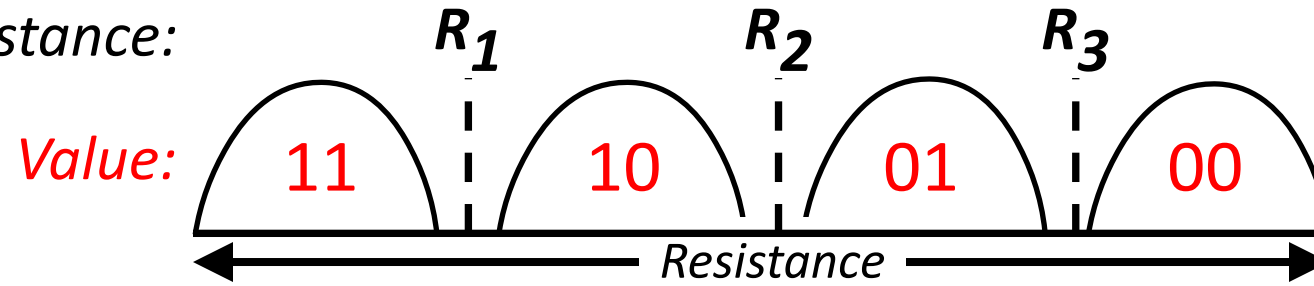


Figure: 2-bit MLC PCM

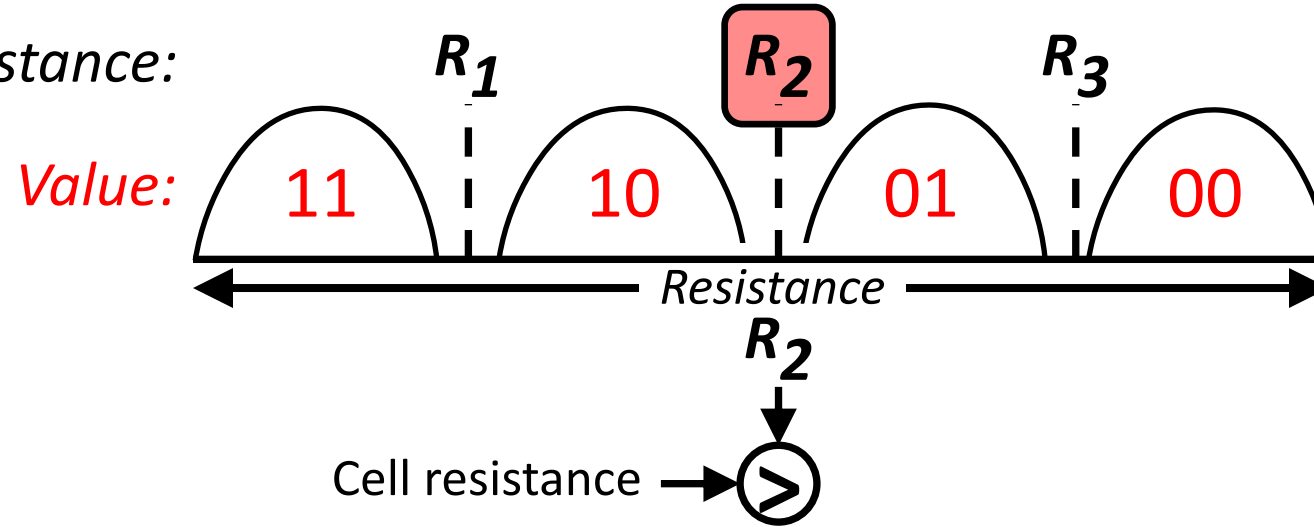
MLC PCM Read Techniques

Reference Resistance:



MLC PCM Read Techniques

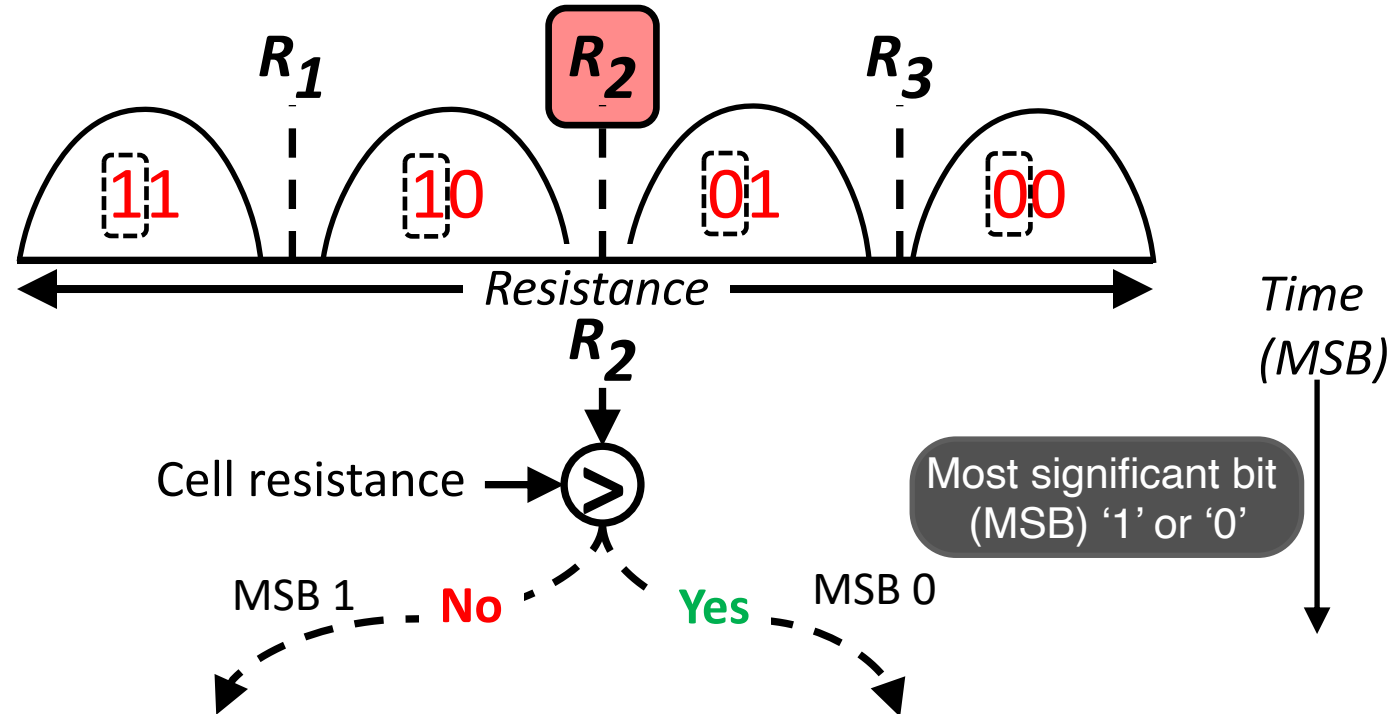
Reference Resistance:



MLC PCM Read Techniques

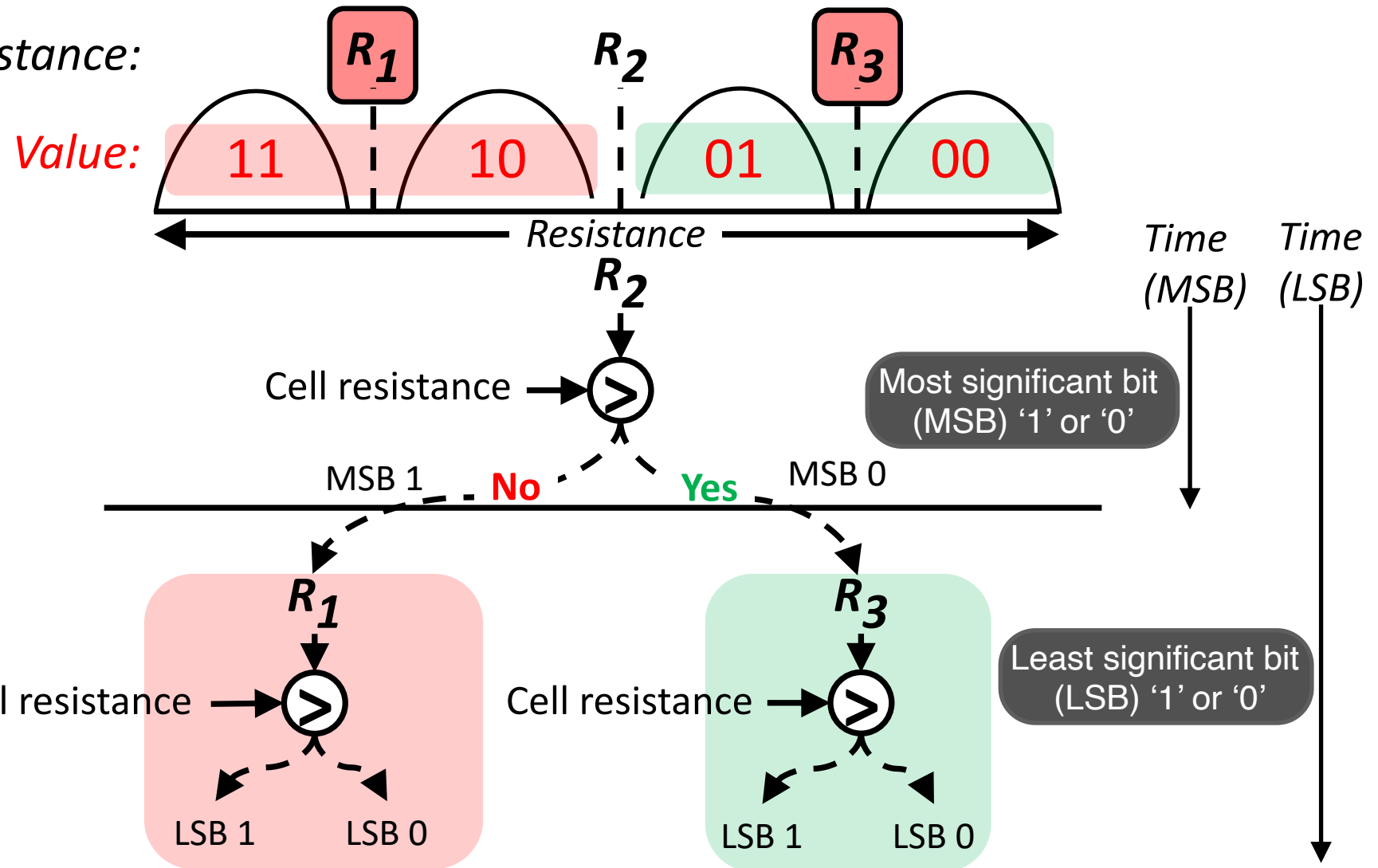
Reference Resistance:

Value:

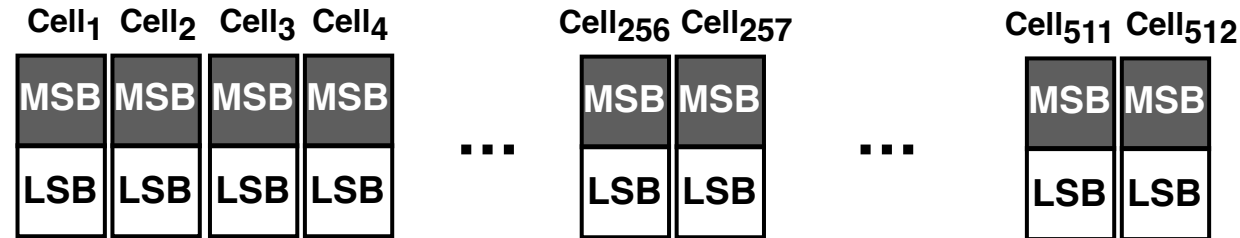


MLC PCM Read Techniques

Reference Resistance:

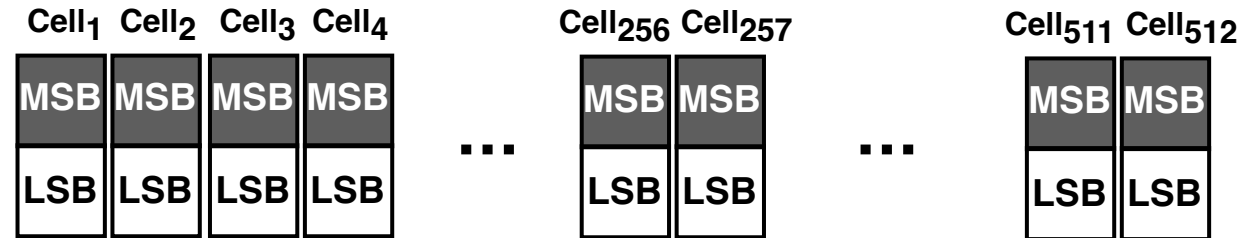


Performance Optimizations for MLC-PCM Reads



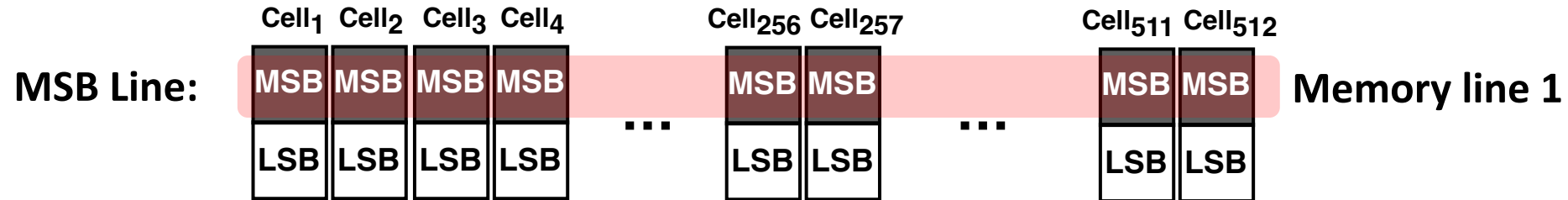
❖ Decouple MSB bit reads from LSB bit reads.

Performance Optimizations for MLC-PCM Reads



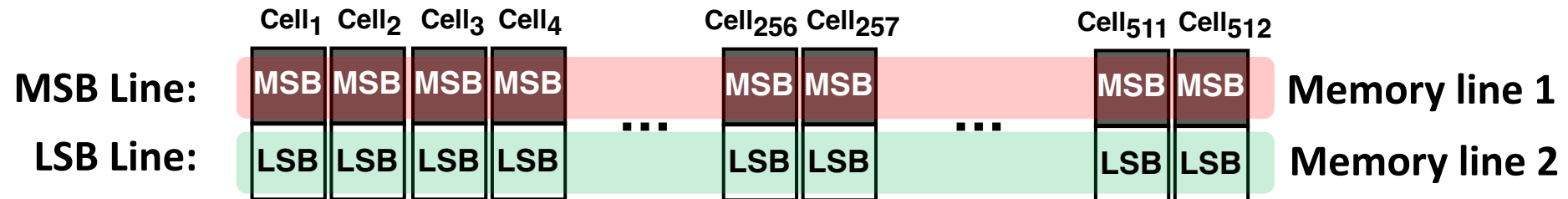
- ❖ Decouple MSB bit reads from LSB bit reads.
- ❖ **Inter-line striping**: Stripe *alternating lines* in different speed grades.

Performance Optimizations for MLC-PCM Reads



- ❖ Decouple MSB bit reads from LSB bit reads.
- ❖ **Inter-line striping:** Stripe *alternating lines* in different speed grades.
 - **MSB Lines:** Memory lines containing *all* MSB bits (faster)

Performance Optimizations for MLC-PCM Reads



- ❖ Decouple MSB bit reads from LSB bit reads.
- ❖ **Inter-line striping:** Stripe *alternating lines* in different speed grades.
 - **MSB Lines:** Memory lines containing *all* MSB bits (faster)
 - **LSB Lines:** Memory lines containing *all* LSB bits (slower)

Are PCM Read Techniques Vulnerable to Leakage?

❖ Microbenchmark:

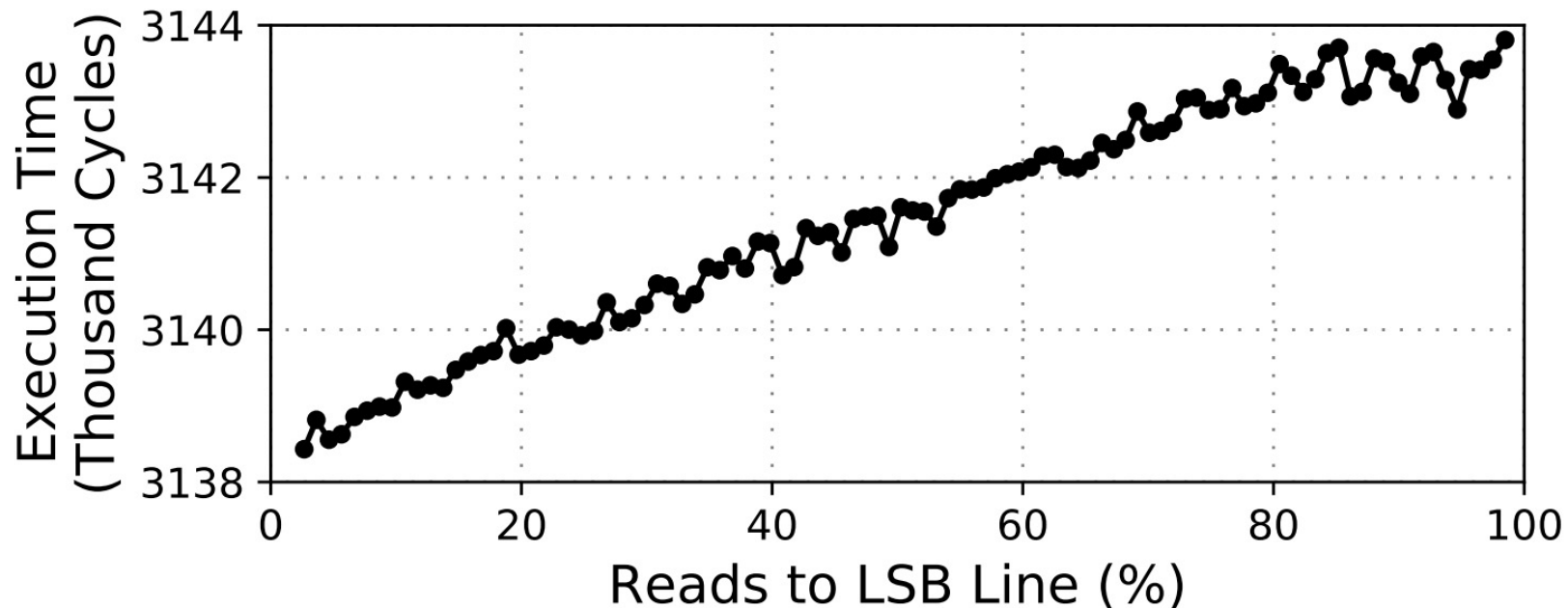
- Issues fixed number of memory accesses
- Varies MSB and LSB lines accesses

Are PCM Read Techniques Vulnerable to Leakage?

❖ Microbenchmark:

- Issues fixed number of memory accesses
- Varies MSB and LSB lines accesses

❖ Increasing LSB ratio -> Deterministic linear increase in execution time

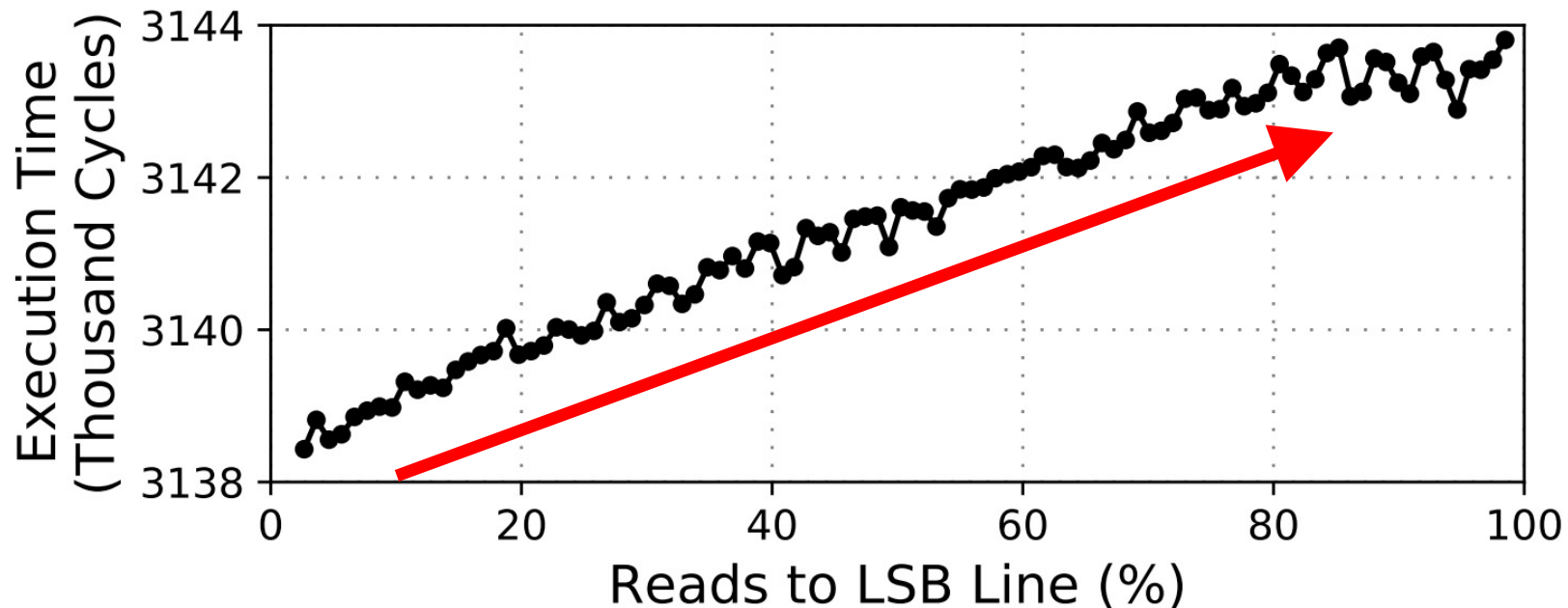


Are PCM Read Techniques Vulnerable to Leakage?

❖ Microbenchmark:

- Issues fixed number of memory accesses
- Varies MSB and LSB lines accesses

❖ Increasing LSB ratio -> Deterministic linear increase in execution time

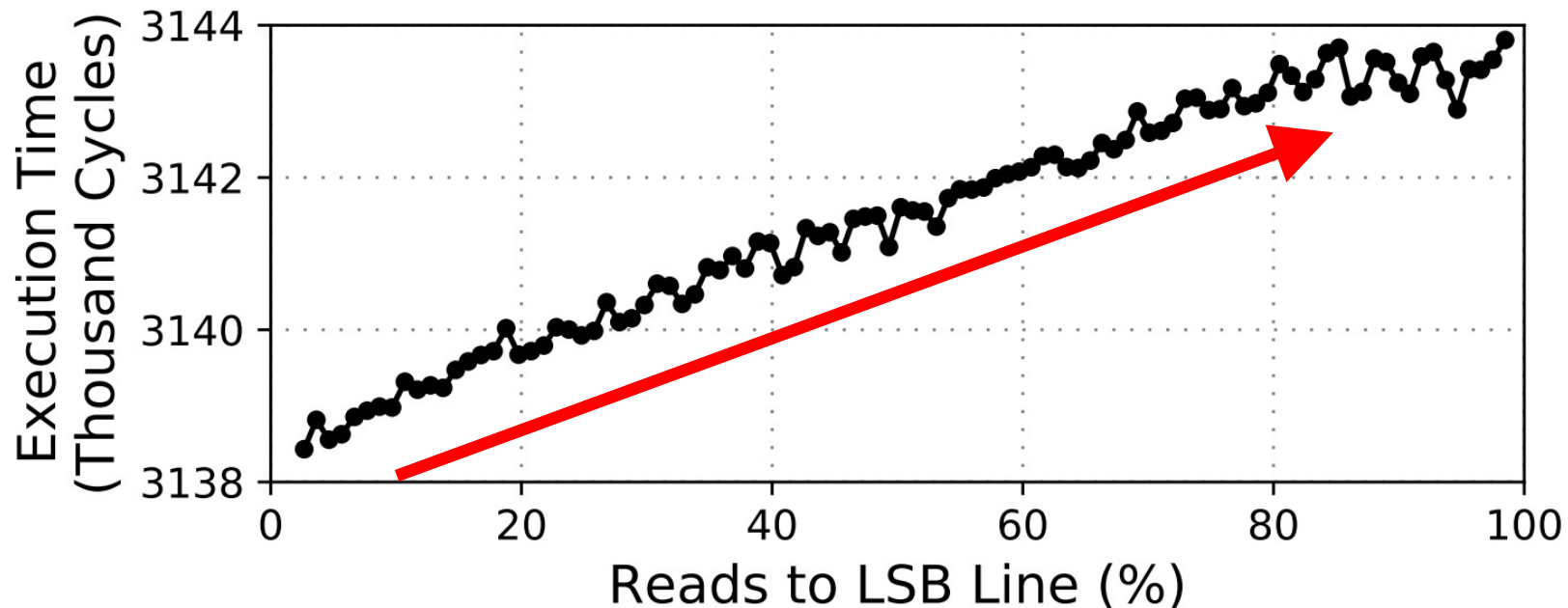


Are PCM Read Techniques Vulnerable to Leakage?

❖ Microbenchmark:

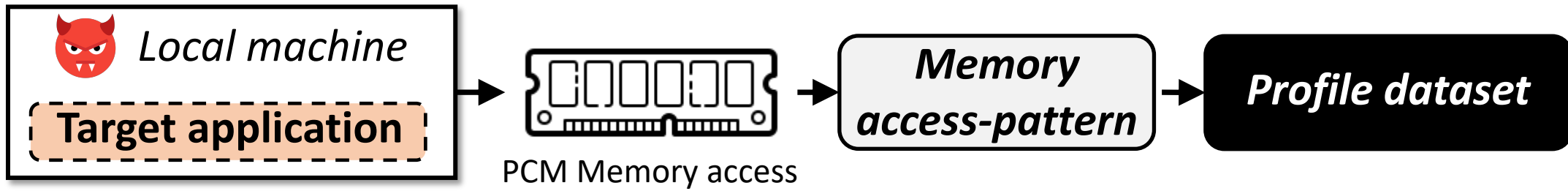
Differentiation in PCM access patterns can induce externally observable slow and fast executions.

❖ Increasing LSB ratio -> Deterministic linear increase in execution time

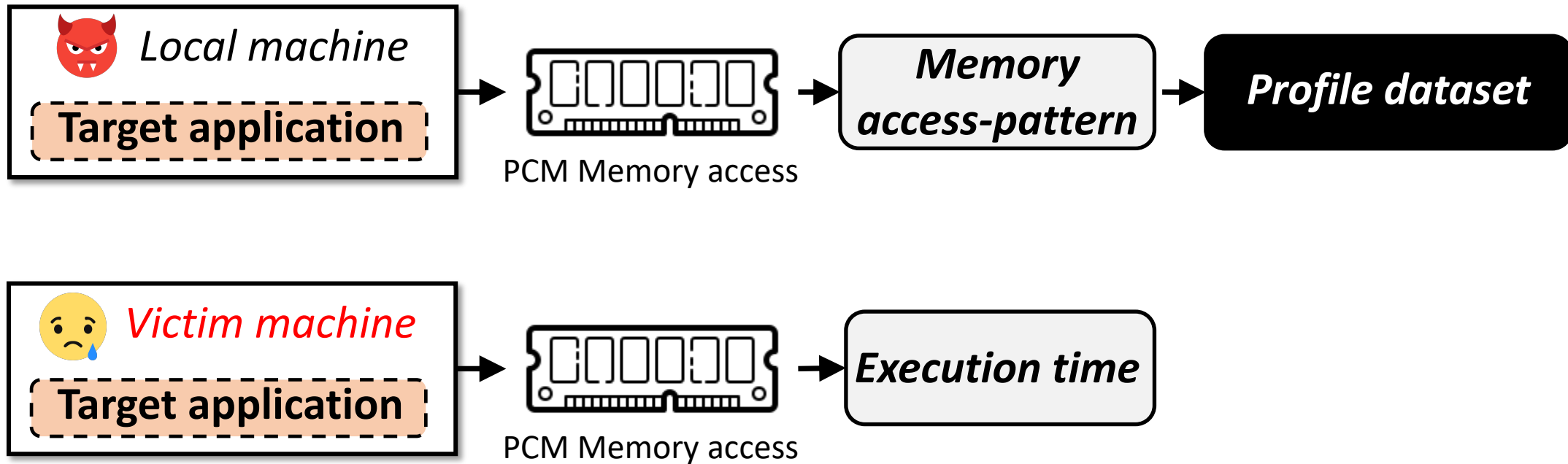


Overview of R-SAW: Exploiting Read Asymmetry

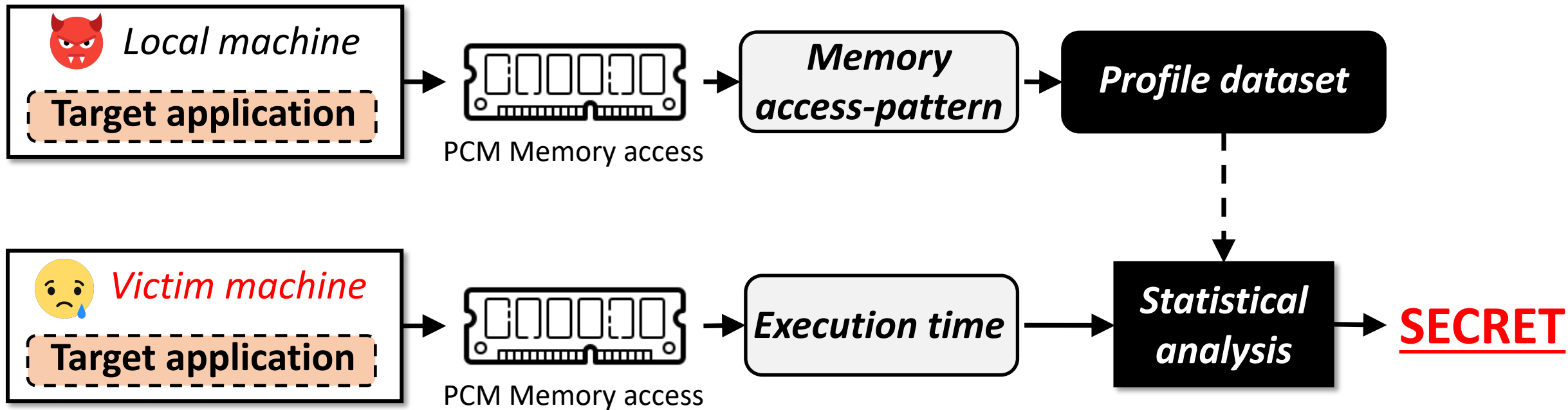
Overview of R-SAW: Exploiting Read Asymmetry



Overview of R-SAW: Exploiting Read Asymmetry

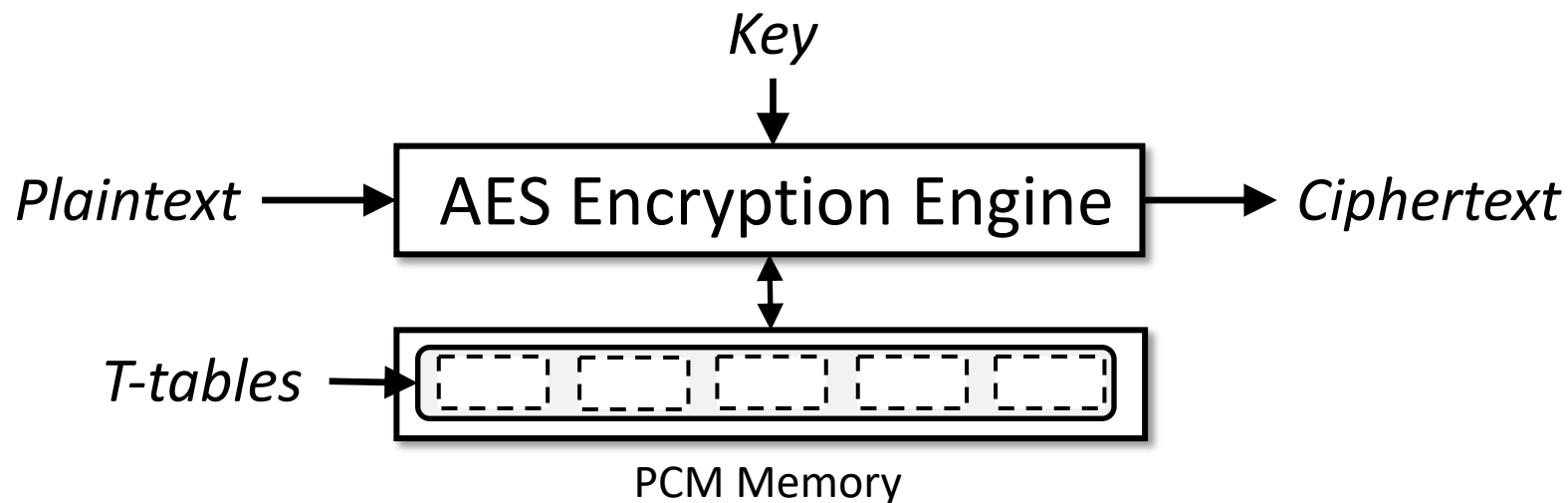


Overview of R-SAW: Exploiting Read Asymmetry



AES Encryption in OpenSSL

- ❖ AES encryption uses pre-computed values from memory (t-tables).
- ❖ PCM access patterns to these t-tables are ***secret key dependent***.



Attacking AES with R-SAW: Offline Profiling

- ❖ Collects **LSB/MSB access ratios (P)** of encryption for random plaintext (PT) and key.
- ❖ Organizes the P based on last round key byte and ciphertext (CT) byte value pair.
- ❖ For each key byte value, **MPV** stores the P corresponding to each CT byte value.

Memory-pattern vector (MPV): $\mathcal{M}(u) = \{\overline{P}_{(u)}^0, \overline{P}_{(u)}^1, \dots, \overline{P}_{(u)}^{255}\}$

Attacking AES with R-SAW: Offline Profiling

- ❖ Collects **LSB/MSB access ratios (P)** of encryption for random plaintext (PT) and key.
- ❖ Organizes the P based on last round key byte and ciphertext (CT) byte value pair.
- ❖ For each key byte value, **MPV** stores the P corresponding to each CT byte value.

Memory-pattern vector (MPV): $\mathcal{M}(u) = \{\overline{P}_{(u)}^0, \overline{P}_{(u)}^1, \dots, \overline{P}_{(u)}^{255}\}$

↑
Last round key byte value, u

↑
LSB Access ratio when $\langle \text{key}, \text{ciphertext} \rangle = \langle u, 255 \rangle$

Attacking AES with R-SAW: Offline Profiling

- ❖ Collects **LSB/MSB access ratios (P)** of encryption for random plaintext (PT) and key.
- ❖ Organizes the P based on last round key byte and ciphertext (CT) byte value pair.
- ❖ For each key byte value, **MPV** stores the P corresponding to each CT byte value.

Memory-pattern vector (MPV): $\mathcal{M}(u) = \{\overline{P}_{(u)}^0, \overline{P}_{(u)}^1, \dots, \overline{P}_{(u)}^{255}\}$

↑
Last round key byte value, u

↑
LSB Access ratio when $\langle \text{key}, \text{ciphertext} \rangle = \langle u, 255 \rangle$

Profile dataset: For each key byte, 256 MPVs corresponding to each value of u

Attacking AES with R-SAW: Runtime Monitoring

- ❖ Attacker monitors **encryption times (L)** for AES encryptions (**unknown key**).
- ❖ Organizes the L based ciphertext byte value.
- ❖ Attacker creates **ETV** by collecting L for each ciphertext byte value.

Encryption-timing vector (ETV): $\mathcal{T}(\mathbf{x}) = \{\overline{L}_{(\mathbf{x})}^0, \overline{L}_{(\mathbf{x})}^1, \dots, \overline{L}_{(\mathbf{x})}^{255}\}$

Attacking AES with R-SAW: Runtime Monitoring

- ❖ Attacker monitors **encryption times (L)** for AES encryptions (**unknown key**).
- ❖ Organizes the L based ciphertext byte value.
- ❖ Attacker creates **ETV** by collecting L for each ciphertext byte value.

Encryption-timing vector (ETV): $\mathcal{T}(\mathbf{x}) = \{\bar{L}_{(\mathbf{x})}^0, \bar{L}_{(\mathbf{x})}^1, \dots, \bar{L}_{(\mathbf{x})}^{255}\}$

Key byte value, **unknown**

Encryption time when $\langle \text{key}, \text{ciphertext} \rangle = \langle \text{unknown}, 255 \rangle$

Attacking AES with R-SAW: Runtime Monitoring

- ❖ Attacker monitors **encryption times (L)** for AES encryptions (**unknown key**).
- ❖ Organizes the L based ciphertext byte value.
- ❖ Attacker creates **ETV** by collecting L for each ciphertext byte value.

Encryption-timing vector (ETV): $\mathcal{T}(\mathbf{x}) = \{\bar{L}_{(\mathbf{x})}^0, \bar{L}_{(\mathbf{x})}^1, \dots, \bar{L}_{(\mathbf{x})}^{255}\}$

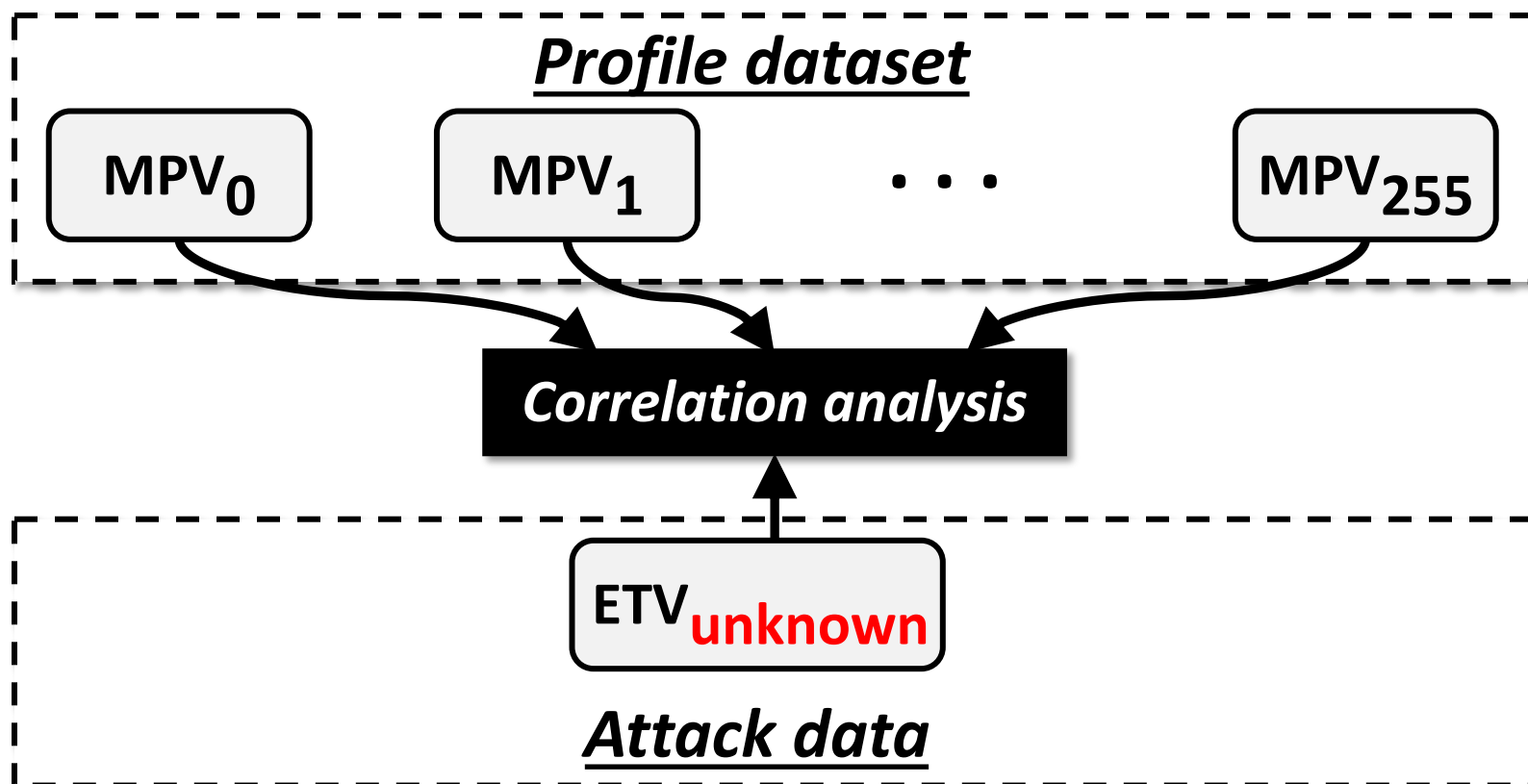
Key byte value, **unknown**

Encryption time when $\langle \text{key}, \text{ciphertext} \rangle = \langle \text{unknown}, 255 \rangle$

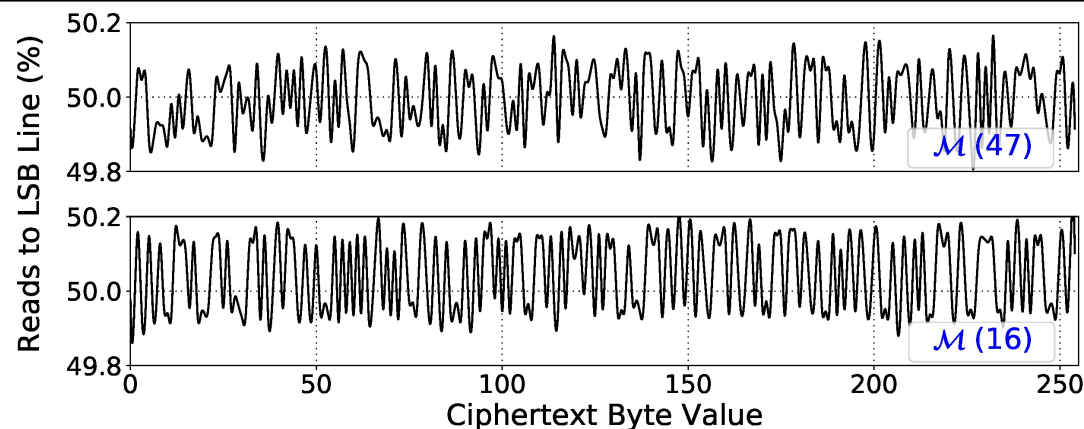
Attack data: One ETV for the key byte value, **unknown**

Attacking AES with R-SAW: Correlation Analysis

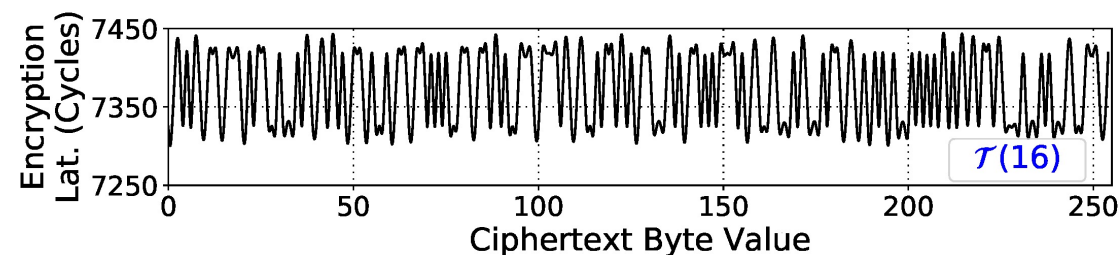
- ❖ Correlation analysis between attack data and profile dataset.
- ❖ Highest and outstanding correlation may indicate the **unknown** key value.



Attacking AES with R-SAW: Evaluation of Attack

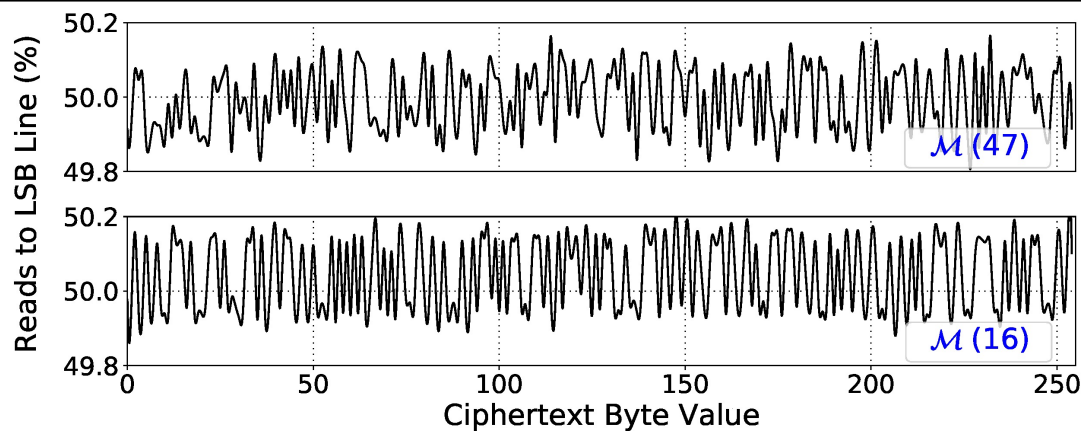


Two example traces of MPV from local system

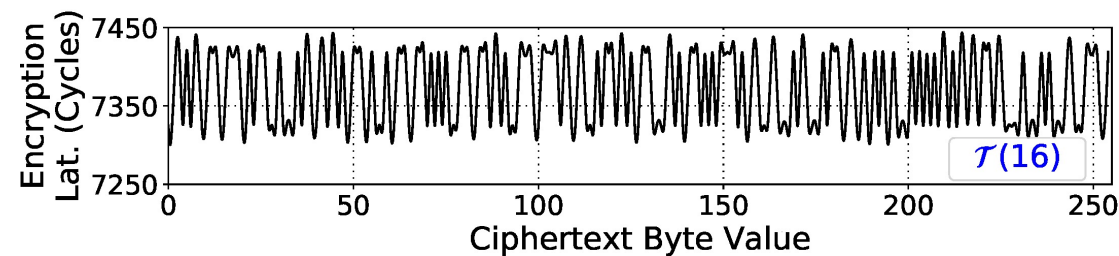


Example ETV from Victim system

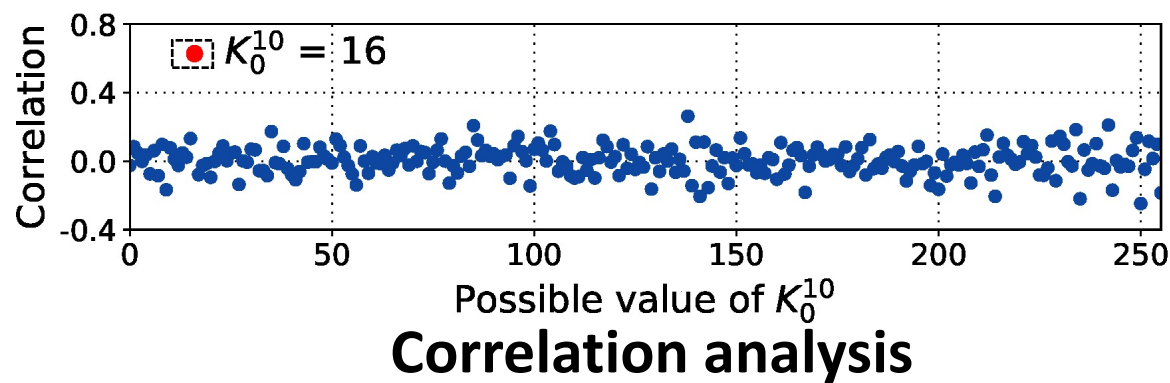
Attacking AES with R-SAW: Evaluation of Attack



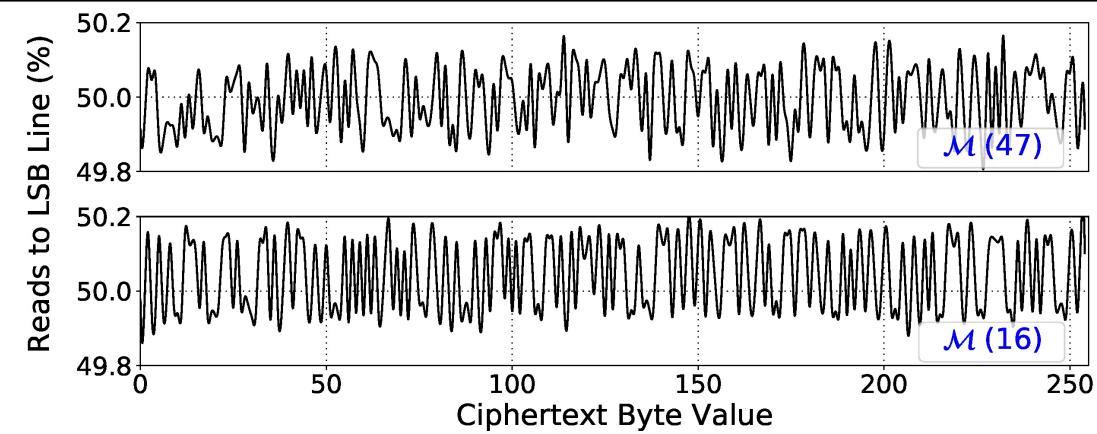
Two example traces of MPV from local system



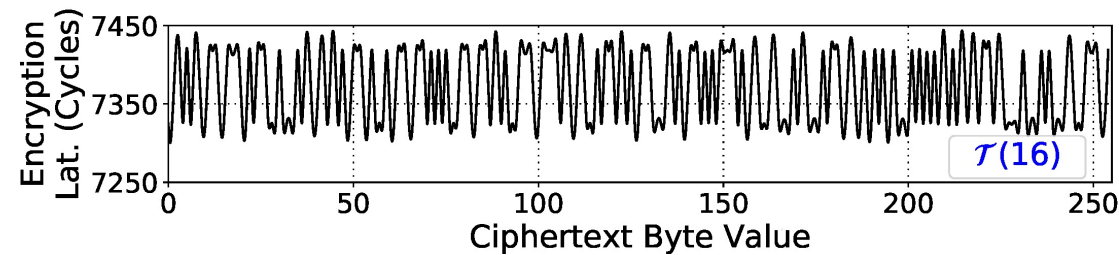
Example ETV from Victim system



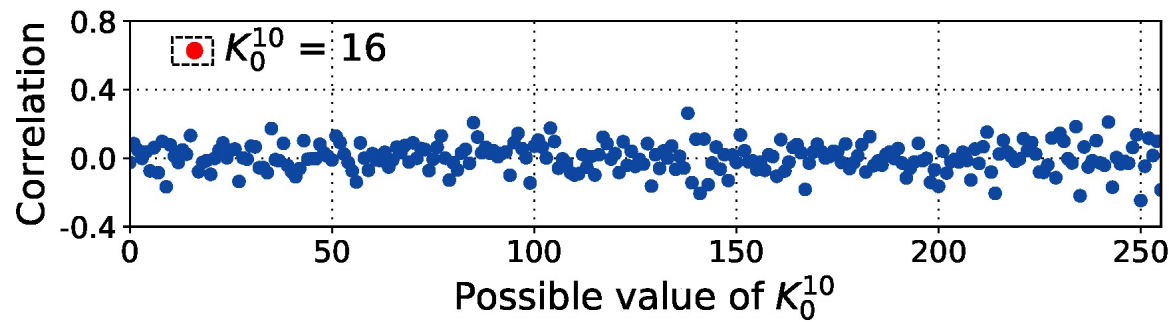
Attacking AES with R-SAW: Evaluation of Attack



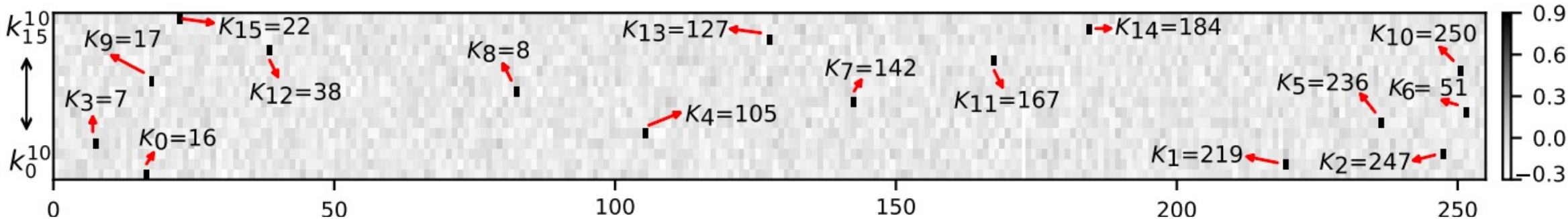
Two example traces of MPV from local system



Example ETV from Victim system

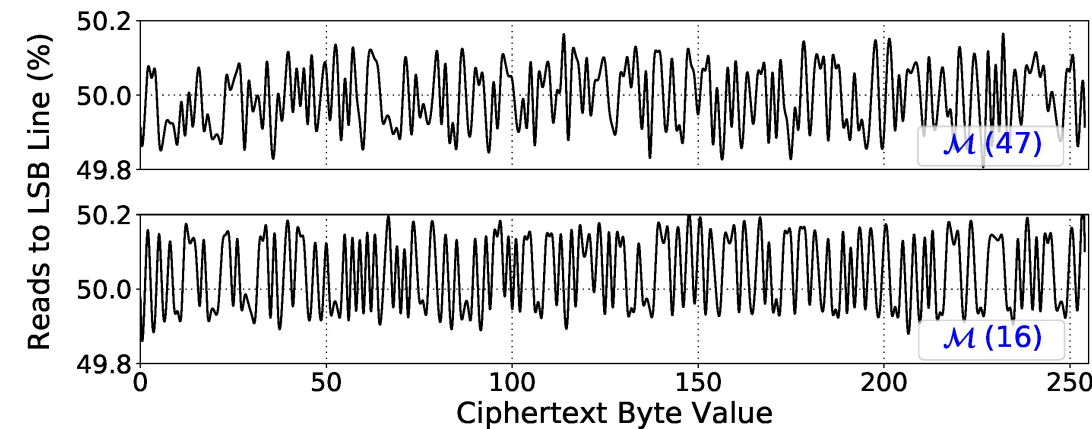


Correlation analysis

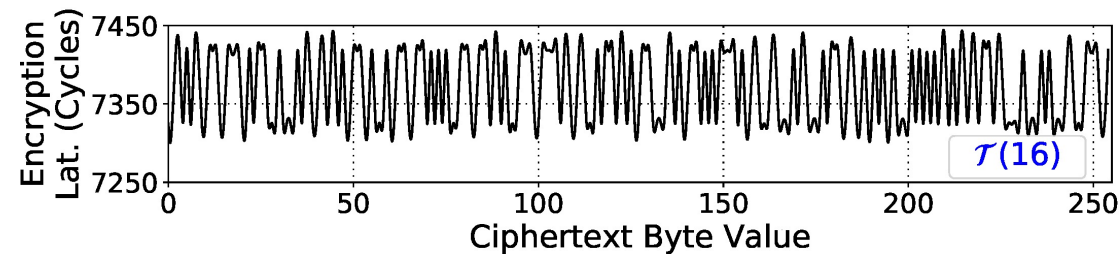


Complete 16-byte AES Key recovery using R-SAW

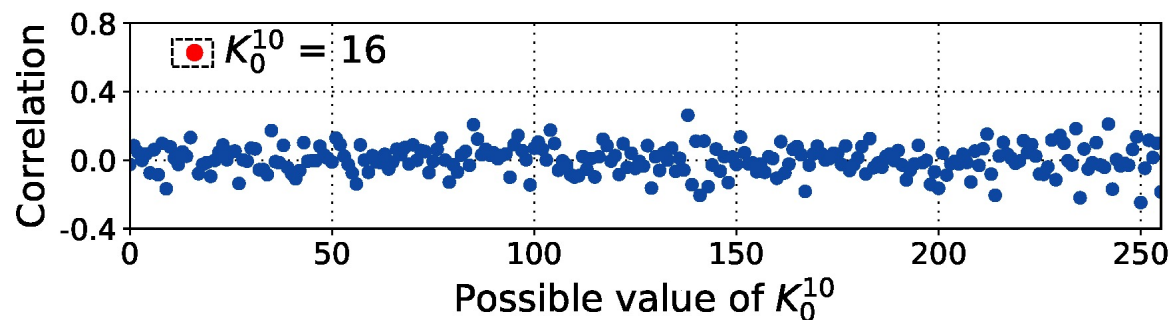
Attacking AES with R-SAW: Evaluation of Attack



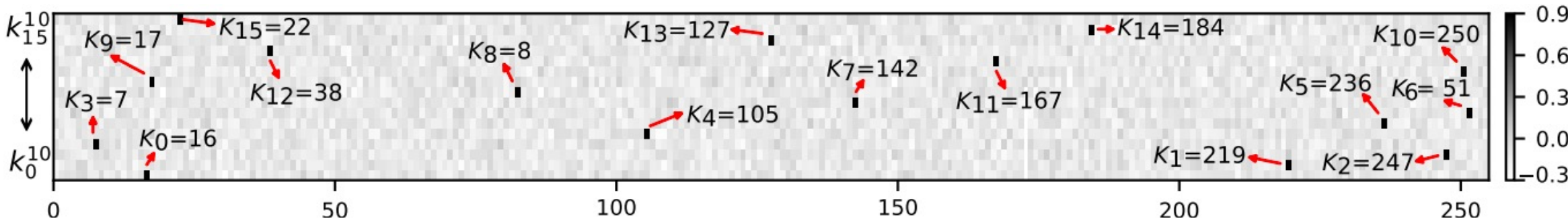
Two example traces of MPV from local system



Example ETV from Victim system



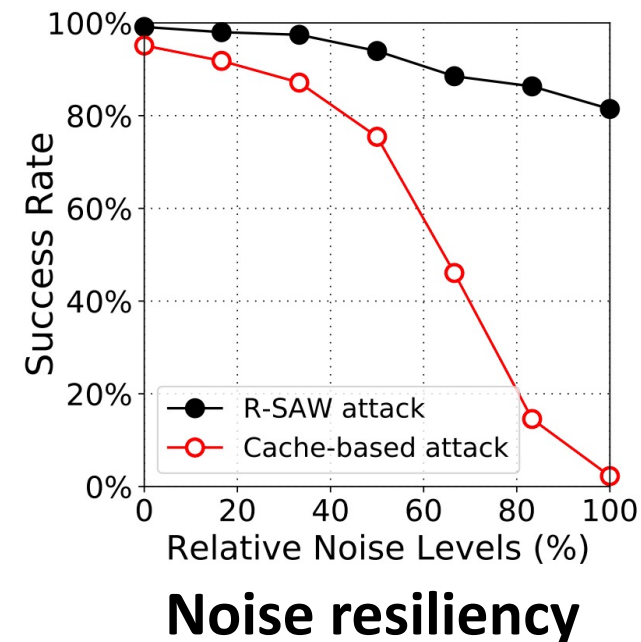
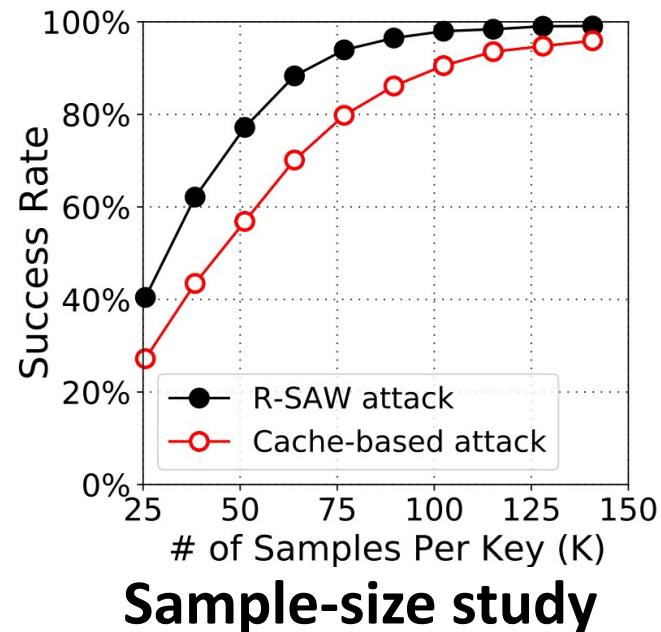
Correlation analysis



Complete 16-byte AES Key recovery using R-SAW

More on paper

- ❖ Comparison of R-SAW with state-of-the-art cache-based attacks.
 - Resiliency of R-SAW against system noise
 - Feasibility of R-SAW with small number of attack samples
- ❖ Discussions on potential mitigations for R-SAW.



Thanks! Questions?

Md Hafizul Islam Chowdhuryy

Email: reyad@knights.ucf.edu